Patent Claims:

1. A method for determining the arrangement of contact areas on the active top side of a semiconductor chip arranged in or on a housing, the method being performed on a computer system and having the following steps of:

a) reading semiconductor chip data into the computer system, the semiconductor chip data comprising geometrical properties of the semiconductor chip (8; 10; 12) and also information about the number of contact areas (811-813; 101-103; 121-123) to be arranged at each edge of the semiconductor chip (8; 10; 12),

b) reading contact area data into the computer system, the contact area data comprising geometrical and electrical properties of the contact areas (811-813; 101-103; 121-123) to be arranged on the active top side (81) of the semiconductor chip (8; 10; 12),

c) reading housing data into the computer system, the housing data comprising geometrical and electrical properties of the housing (7) and also of the contact pads (721-723) arranged on the top side of the housing (7),

d) reading production data into the computer system, the production data defining the arrangement of the semiconductor chip (8; 10; 12) in relation to the housing (7), ,

e) generating a model of an electronic device (6; 9; 11), which comprises the housing (7) and the semiconductor chip (8; 10; 12) arranged with its passive rear side on the top side of the housing (7), from the data read in in steps a) to d),

f) arranging the contact areas (811-813; 101-103; 121-123) in the model of the electronic device (6; 9; 11) in edge regions on the active top side (81) of the semiconductor chip (8; 10; 12) in such a

way

- that the contact areas (811-813) in each case lie on straight connecting lines between the contact pads (721-723) within the housing (7) and the area centroid (82) of the active top side (81) of the semiconductor chip (8), or
- that, in the case of contact areas (101-103) arranged at a respective semiconductor chip edge, distances (d) of identical magnitude in each case are provided between adjacent contact areas (101-103) and/or between the respective outermost contact areas (101, 103) per semiconductor chip edge and the adjoining semiconductor chip edges, or
- that the contact areas (811-813) are firstly in each case arranged on connecting lines between the contact pads (721-723) on the top side of the housing (7) and the area centroid (82) of the active top side (81) of the semiconductor chip (8), and that the contact areas (101-103) arranged at an identical semiconductor chip edge are subsequently displaced such that the distances (d) between adjacent contact areas (101-103) and/or between the respective outermost contact areas (101, 103) per semiconductor chip edge and the adjoining semiconductor chip edges are formed with the same magnitude in each case, or
- that the distances between the contact areas (121-123) and contact pads (721-723) that are to be electrically connected to one another in each case are minimized,

g) providing the contact area arrangement data, which comprise information about the arrangement - determined in step f) - of the contact areas (811-813; 101-103; 121-123) on the active top side (81) of the semiconductor chip (8; 10; 12), for subsequent fabrication and/or design processes of

the semiconductor chip (8; 10; 12) and/or of the housing (7) and/or of the electronic device (7; 9; 11).

2. A method for creating a bonding plan for an electronic device having a semiconductor chip and having a housing, which is performed on a computer system and has the following steps of:

a) determining the arrangement of contact areas (121-123) on the active top side (81) of the semiconductor chip (12) by performing the method as claimed in claim 1,

b) determining the arrangement of integrated circuits (CPU, RAM, FLASH, EEPROM) on the active top side (81) of the semiconductor chip (8; 10; 12) and/or of filler structures (131-133), which ensure the electrical connection between the contact areas (121-123) and are arranged at the edge of the active top side (81) of the semiconductor chip (12) in each case between the contact areas (121-123),

c) determining a model of the active top side (12) of the semiconductor chip (12), the semiconductor components of the integrated circuits (CPU, RAM, FLASH, EEPROM) determined in step b) being defined, positioned and wired in the model at the gate level, and the model having a plurality of levels arranged above and next to one another,

d) checking the electrical and the logical behavior of the semiconductor chip (12) on the basis of the model determined in step c) using simulation and verification methods,

e) extracting the data required for the bonding plan from the model determined in step c),

f) reading in housing data, which comprise geometrical and/or electrical properties of the housing (7) and also of the contact pads (721-723) arranged on the top side of the housing (7), into

the computer system,

g) creating a bonding plan on the basis of the data extracted in step e) and on the basis of the housing data read in in step f), the bonding plan comprising a model of the housing (7) and of the semiconductor chip (12) arranged in or on the housing (7) and also a representation of the bonding connections between the contact areas (121-123) and the contact pads (721-723),

h) checking the bonding plan created in step g) for alterations with respect to the model of the electronic device generated in step a), in particular for deletions, for combinations and for interchangings of the contact areas (121-123),

i) providing the bonding plan for the bonding machines.

3. A method for generating geometry data for the creation of photomasks for the exposure of an electronic device having a semiconductor chip and having a housing by means of photolithographic methods, the method being formed on a computer system and having the following steps of:

a) determining the arrangement of contact areas (121-123) on the active top side (81) of the semiconductor chip (12) by performing the method as claimed in claim 1,

b) determining the arrangement of integrated circuits (CPU, RAM, FLASH, EEPROM) on the active top side (81) of the semiconductor chip (8; 10; 12) and/or of filler structures (131-133), which ensure the electrical connection between the contact areas (121-123) and are arranged at the edge of the active top side (81) of the semiconductor chip (12) in each case between the contact areas (121-123),

c) determining a model of the active top side (81) of the semiconductor chip (12), the semiconductor

components of the integrated circuits (CPU, RAM, FLASH, EEPROM) determined in step b) being defined, positioned and wired at the gate level in the model, and the model having a plurality of levels arranged above and next to one another,

d) checking the electrical and the logical behavior of the semiconductor chip (12) on the basis of the model determined in step c) using simulation and verification methods,

e) determining the geometry data required for the photomasks from the model of the active top side (81) of the semiconductor chip (12) determined in step c), with production tolerances being included in the calculation,

f) checking the geometry data generated in step e) for alterations with respect to the model of the electronic device (11) generated in step a), in particular for displacements, for deletions, for combinations and for interchangings of the contact areas (121-123),

g) providing the geometry data generated for the subsequent creation of the photomasks.

4. A semiconductor chip, the fabrication of which has involved performing a method as claimed in one of claims 1 to 3.

5. An electronic device having a housing and having a semiconductor chip arranged in or on the housing, the fabrication of the electronic device and/or of the housing and/or of the semiconductor chip having involved performing a method as claimed in one of claims 1 to 3.

6. A housing for a semiconductor chip, the fabrication of which has involved performing a method as claimed in claim 1.

7. A computer program product and a computer program for performing a method for determining the arrangement of contact areas on the active top side of a semiconductor chip, which is configured such that a method as claimed in claim 1 can be performed.

8. A computer program product and a computer program for performing a method for creating a bonding plan for an electronic device having a semiconductor chip and having a housing, which is configured such that a method as claimed in claim 2 can be performed.

9. A computer program product and a computer program for performing a method for generating geometry data for the creation of photomasks for the exposure of an electronic device having a semiconductor chip and having a housing by means of photolithographic methods, the method being configured such that a method as claimed in claim 3 can be performed.

10. The computer program as claimed in one of claims 7 to 9, which is stored on a storage medium or in a computer memory, in particular in a random access memory.

11. The computer program as claimed in one of claims 7 to 9, which is transmitted on an electrical carrier signal.

12. A data carrier having a computer program as claimed in one of claims 7 to 9.

13. A method in which a computer program product or computer program as claimed in one of claims 7 to 9 is downloaded from an electronic data network such as from the Internet, for example, onto a computer connected to the data network.